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10/538,806	06/28/2005	Simon Tam	124280	5681
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OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850				RAINEY, ROBERT R
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/538,806	TAM, SIMON	
	Examiner	Art Unit	
	ROBERT R. RAINY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 March 2010.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 12-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 12-23 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 13 June 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application

6) Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 12-23 have been considered but are moot in view of the new ground(s) of rejection. However, inasmuch as some of the arguments may apply to the new grounds of rejection examiner offers the following comment. Arguments regarding whether or not it would have been obvious to practice the claimed invention in the context of any particular application/device are not generally ripe for consideration while the claims do not tie the invention to the particular application/device.

Claim Rejections - 35 USC § 103

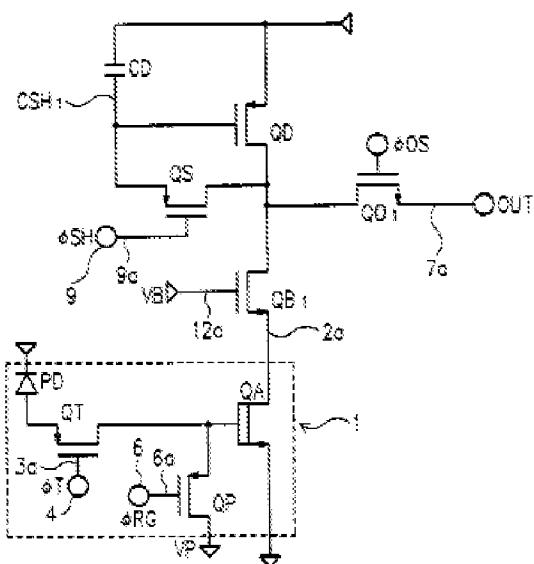
2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 12-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. U.S. Patent No. 5,933,189 to *Nomura* ("Nomura").

As to **claim 12**, Nomura discloses a solid-state image pickup apparatus and in particular a differential circuit comprising:

Fig. 8



a first transistor that has a first drain and a first source (see for example Fig. 8 "QD");

a capacitor that is connected to a first gate of the first transistor (see for example Fig. 8 "CD");

a first switch that controls an electrical connection between the first gate and the first drain (see for example Fig. 8 "QS");

a second transistor that has a second drain and a second source and is connected to the first transistor (see for example Fig. 8 "QA"); and

a second switch (see for example Fig. 8 "QP"), and a third switch (see for example Fig. 8 "QT") ~~and a fourth switch~~ respectively applying first (see for

example Fig. 8 "VP"), and second (see for example Fig. 8 the voltage applied by the PD circuit) ~~and third~~ independent voltages to a second gate of the second transistor,

the differential circuit being configured such that in a first period the first gate is electrically connected to the first drain through the first switch and the first independent voltage is applied to the second gate through the second switch (see for example Fig. 5, especially time period T11 in which signals RG and SH activate transistors QP and QS respectively; note that the discussion of the operation of the elements using Fig. 5 is made with respect to Fig. 3 and 4 and common elements in later embodiments are referenced back to the original description. Nomura seems to have made an inadvertent change of QS polarity between Fig. 4 and Fig. 8 so Fig. 4 must be referenced in order to see the operation of the two modes with QS and QP on to charge the capacitor then QT on to perform the current comparison.),

in a second period the second independent voltage is applied to the second gate through the third switch (see for example Fig. 5, especially time period T13 in which signal T1 activates transistor QT), and

~~none of~~ the first and second and third periods not overlapping (see for example Fig. 5).

Nomura discloses the claimed invention except for a fourth switch applying a third independent voltage to a second gate of the second transistor; and

in a third period the third independent voltage is applied to the second gate through the fourth switch,

none of the first, second and third periods overlapping.

Multiplexers, i.e. multiple switches, each being operated by a drive signal which is independent of and non-overlapping with drive signals applied to the other switches and each operably applying an independent voltage to a detection element, were well known to those skilled in the art at the time of the invention.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to duplicate the PD-QT pair and provide signals appropriate to multiplex any desired number of independent voltages into the detection node, i.e. the gate of QA. The suggestion/motivation would have been to provide advantages such as to reduce the required number of detection circuits.

13. The differential circuit according to claim 12, wherein the differential circuit is configured such that a first current flows through the first transistor and the second transistor during the first period (see for example Fig. 5 and 8).

14. The differential circuit according to claim 12, wherein the differential circuit is configured such that a second current flows through the first transistor and the second transistor during the second period (see for example Fig. 5 and 8).

15. The differential circuit according to claim 12, wherein the differential circuit is configured such that the second transistor functions as a current source (see for example 8).

As to **claim 16**, in addition to the rejection of claim 12 over *Nomura*: discloses the claimed invention except for the circuit being configured such that the first switch and the second switch are controlled by an identical signal.

At the time of the invention, there was a recognized need in the art to cause two switches to conduct at the same time. Note that this is the case in *Nomura*: in order to program the upper current source of figure 8 both QS and QP must be conducting at the same time.

There were a finite number of identified, predictable potential solutions to the recognized need or problem. In this case the finite number is two. The activation of multiple switches by an identical signal was well known and thus its effect would be predictable. And *Nomura* taught the second alternative, which is to drive the switches with non-identical signals with overlapping activation

portions - in order to program the upper current source of figure 8 both QS and QP must be conducting at the same time.

One of ordinary skill in the art could have pursued the known potential solutions with a reasonable expectation of success. Since both options were known and the complexity of the implementation would be low, the expectation of success would be very high.

A further indicator of obviousness is that one of ordinary skill would have been motivated by design forces driving reduced component and trace count to implement identical signal driving. These forces manifest in every design. Even if it they are sometimes overridden by other concerns, their influence is still evident since reduced component and trace count lead to multiple benefits such as reduced cost, reduced size, and greater reliability.

As to **claim 17**, in addition to the rejection of claim 12 over *Nomura*, *Nomura* further discloses an amplifier that is connected to the first transistor (see for example Fig. 3 item 8).

As to **claim 18**, in addition to the rejection of claim 12 over *Nomura*, *Nomura* further discloses that any one of the second drain and the second source is electrically connected to a predetermined potential (see for example

Fig. 8 in which QA is connected to a predetermined potential represented by the triangle).

As to **claim 19**, in addition to the rejection of claim 13 over *Nomura*, *Nomura* further disclose that the differential circuit is configured such that a charge corresponding to the first current is charged to the capacitor during the first period (see for example Fig. 5 and 8).

As to **claim 20**, in addition to the rejection of claim 12 over *Nomura*, *Nomura* further discloses that differential circuit is configured such that the differential circuit amplifies an output of a sensor pixel (see for example Fig. 5 especially item PD; note however that without further limitation this claim merely says that it amplifies something – “sensor pixel” by itself doesn’t convey much structure).

As to **claim 21**, in addition to the rejection of claim 12 over *Nomura*, since a differential circuit is an electronic device the limitation was covered in the rejection of claim 12.

As to **claim 22**, in addition to the rejection of claim 12 over *Nomura*:

Note that the differential circuit of *Nomura* is a type of auto-zero amplifier.

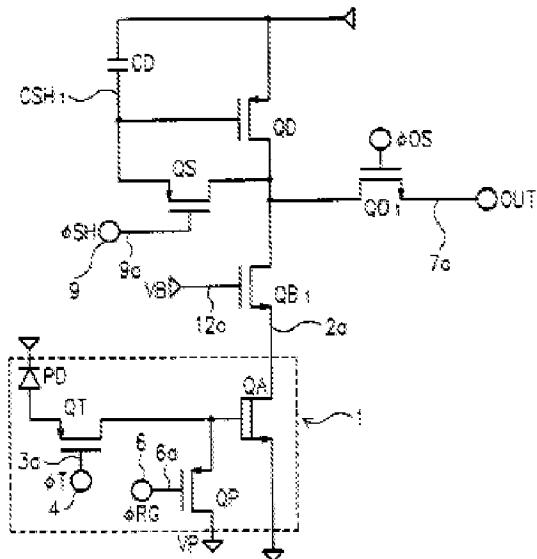
Nomura further discloses a first period being provided before each measurement period (see for example Fig. 5), which by extension to the combination as presented leads to a case in which a first period is provided between each of the second and third periods.

Further, since there is only one other option, namely to not provide a first period between each of the second and third periods, one of ordinary skill could have pursued the options with a reasonable expectation of success since the trade-offs between more and less frequent auto-zero cycles would have been apparent to one of ordinary skill.

4. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. U.S. Patent No. 5,933,189 to *Nomura* (“*Nomura*”) in view of U.S. Patent No. 6,667,767 to *Muramatsu et al.* (“*Muramatsu*”) and further in view of U.S. Patent No. 6,421,085 to *Xu* (“*Xu*”).

As to **claim 23**, *Nomura* discloses a solid-state image pickup apparatus and in particular a differential circuit comprising:

Fig. 8



a first transistor that has a first drain and a first source (see for example Fig. 8 "QD");

a capacitor that is connected to a first gate of the first transistor (see for example Fig. 8 "CD");

a first switch that controls an electrical connection between the first gate and the first drain (see for example Fig. 8 "QS");

a second transistor that has a second drain and a second source (see for example Fig. 8 "QA");

~~a second switch, and a third switch that are connected in parallel and control an electrical connection between the first transistor and the second transistor; and~~

a fourth switch (see for example Fig. 8 "QP") and a fifth switch (see for example Fig. 8 "QT") respectively applying first (see for example Fig. 8 "VP") and second (see for example Fig. 8 the voltage applied by the PD circuit) independent voltages to a second gate of the second transistor,

the differential circuit being configured such that in a first period the first gate is electrically connected to the first drain through the first switch, the first transistor is electrically connected to the second transistor ~~through the second switch~~ and the first independent voltage is applied to the second gate through the fourth switch (see for example Fig. 5, especially time period T11 in which signals RG and SH activate transistors QP and QS respectively; note that the discussion of the operation of the elements using Fig. 5 is made with respect to Fig. 3 and 4 and common elements in later embodiments are referenced back to the original description. Nomura seems to have made an inadvertent change of QS polarity between Fig. 4 and Fig. 8 so Fig. 4 must be referenced in order to see the operation of the two modes with QS and QP on to charge the capacitor then QT on to perform the current comparison.), and

in a second period the first transistor is electrically connected to the second transistor ~~through the third switch~~ and the second independent voltage is applied to the second gate through the fifth switch (see for example Fig. 5, especially time period T13 in which signal T1 activates transistor QT),

the first and second periods being non-overlapping (see for example Fig. 5).

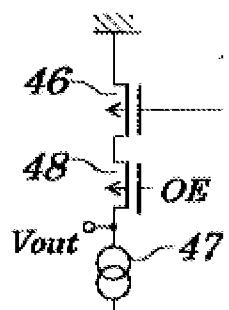
Nomura does not expressly disclose a second switch, and a third switch that are connected in parallel and control an electrical connection between the first transistor and the second transistor; and

in a first period the first transistor being electrically connected to the second transistor through the second switch, and

in a second period the first transistor being electrically connected to the second transistor through the third switch.

Muramatsu discloses an image sensor for offsetting threshold voltage of a transistor in a source follower and in particular:

An output enable switch, i.e. second switch, (see for example figure 6 item 48 driven by signal OE) connected between a current source, i.e. first transistor, (see for example figure 6 at least item 46) and an output node (see for example figure 6 item Vout), which output node is also connected to a second current source, i.e. second transistor, (see for example figure 6 item 47).



It was well known that an output enable switch is driven to enable its connection only when the connection is advantageous and disable it when it is not, that is when having the connection made would cause unnecessary power use or unpredictable or adverse circuit performance.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to add an output enable switch, i.e. second switch, as taught by *Muramatsu* to the circuit of *Nomura*, such that the first transistor is electrically connected to the second transistor through the second switch and to use the switch to break the connection when connection is not advantageous, which is when the state of QA would be indeterminate (if neither QT nor QP is active the state of QA is indeterminate and thus the output is not valid).

Nomura and *Muramatsu* are analogous art because they are from the same field of endeavor, which is current-source-based amplifiers.

The suggestion/motivation would have been to provide advantages such as to reduce power use or to prevent adverse circuit performance.

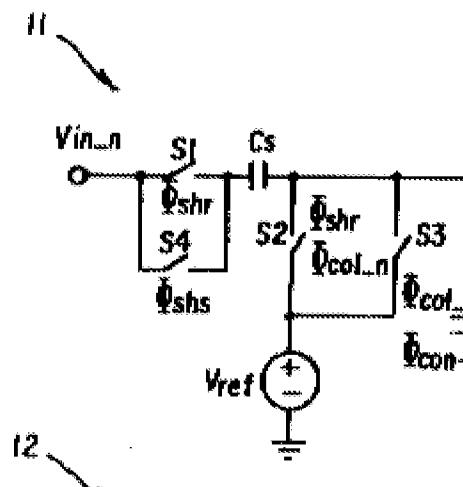
Nomura and *Muramatsu* do not expressly disclose a third switch connected in parallel with the second switch and;

in a first period the first transistor being electrically connected to the second transistor through the second switch, and

in a second period the first transistor being electrically connected to the second transistor through the third switch.

However, it would have been obvious to one of ordinary skill in the art to implement the claimed modification through the use of a known technique that had been used to improve similar devices.

Xu discloses a high speed CMOS imager column CDS circuit, and in particular a comparable device (see for example figure 2 item Vref)



that has been improved in the same way as the claimed invention, that is in a first period the comparable device being electrically connected to its load through the second switch, and in a second period the comparable device being electrically connected to its load through the third switch (see for example figure 2 parallel switches S2 and S3 which are driven by independent signals timed according to figure 3).

One of ordinary skill in the art could have applied the known improvement technique of *Xu* in the same way to the device of *Nomura* and *Muramatsu* and

the results would have been predictable to one of ordinary skill in the art (since Muramatsu already taught the effect of one switch the effect of an additional switch driven by another signal would have been very predictable).

A further evidence of obviousness is that not only are the improved devices comparable but *Xu* and *Nomura* as modified by *Muramatsu* are also from the same field of endeavor, which is image pickup devices.

And as yet further evidence of obviousness consider that while examiner has offered the rejection based on art and arguments that read on applicant's disclosed invention. The claimed second and third switches are also obvious since they can be read on wires or always-on switches since there is no requirement that either of them cease conduction. Two wires could be used for redundancy or impedance matching or always-on switches could be used for impedance, capacitance, offset voltage or temperature compensation.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sharpe-Geisler et al., U.S. Patent No. 5568066, Fig. 7 teaches the use of multiple switches arranged in parallel to create a logical-OR function of n independent signals to control the connection of a source to a load. (evidence of a known technique)

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629